EE 391 (All Sec

Midterm Examination

Tuesday, October 28, 2003

7:00 PM

Time Allowed: 2 Hours

Materials allowed: Laboratory Notebooks, Calculators

Instructions:

- **Answer all questions in the space provided (use page backs for rough work if necessary)**
- **State your assumptions; show all relevant work. Box, circle or otherwise highlight your answers where appropriate. For multiple choice, circle the correct answer.**
- **Put your <u>name</u> and <u>student number</u> on each page; (we may separate them for marking purposes)**
- **Refer to the last page for relevant product data when required**
- **Weighting for each question is indicated in the left margin (Total marks: 120)**

(Marker's use only.)

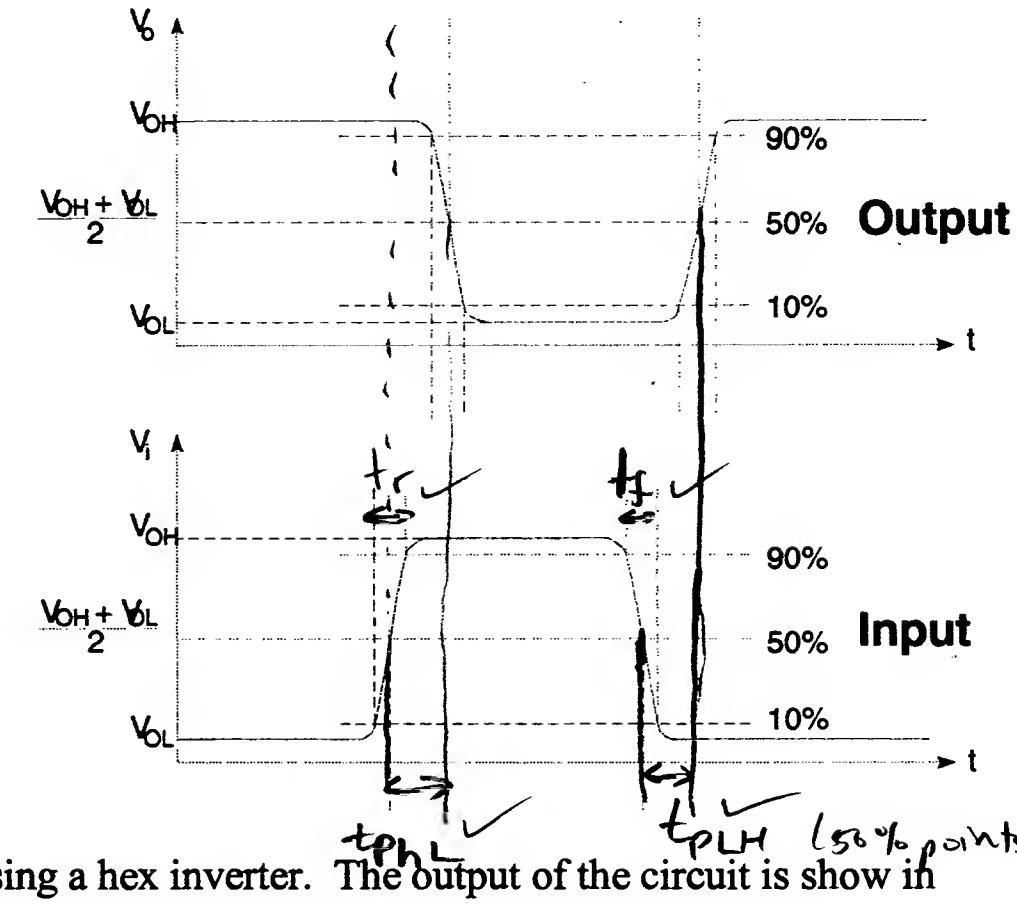
S. L.	BJT	2nd Ord	Fourier	Op A	FET	Total
19 /19	21 /22	20 /21	16 /20	19 /20	10.5 /18	105.5 /120

Name: Chris Mullens

Student Number: 3214111

Timing in Sequential Logic

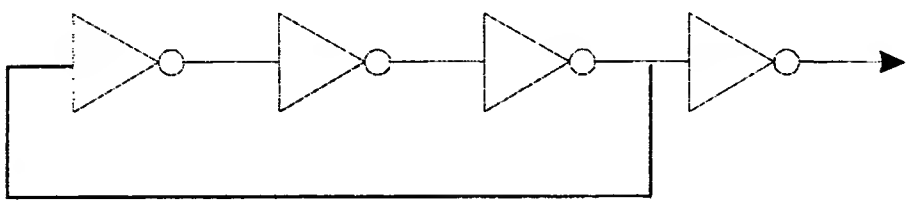
[4] 1.1).The sketch at right show the input and output waveforms for a logic gate (inverter). On this sketch indicate the propagation delays, t_{PHL}, t_{PLH}, the rise time, t_r, and the fall time, t_f.

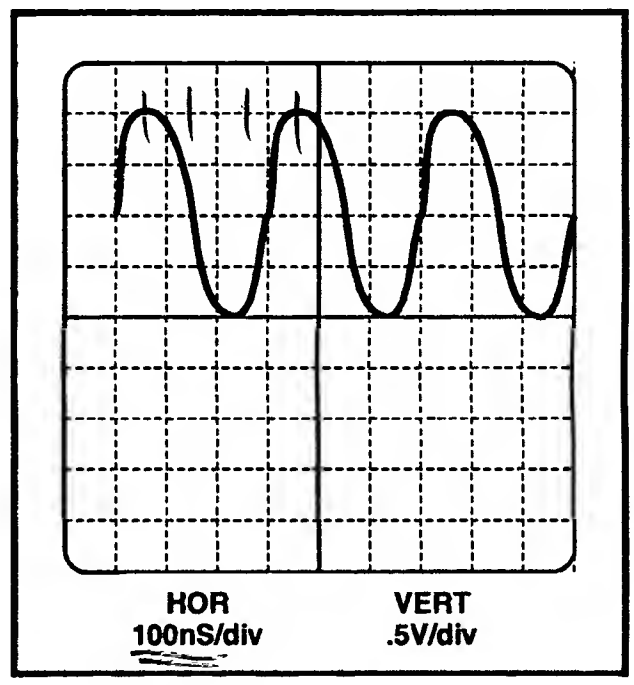


(50% points)

4

[4] 1.2) The following circuit is setup using a hex inverter. The output of the circuit is show in the oscilloscope trace at right. Estimate the average propagation delay for one of the inverters.





$T = 3 \text{ divisions} * 100\text{ns/div}$

$= 300\text{ns}$

$t_p = \frac{T}{2(N)} \qquad t_p = \frac{300\text{ns}}{2(3)}$

$t_p = 50\text{ns}$

4

[1] 1.3) The Power Delay Product (PDP) is used as a figure of merit to compare logic families. It can be defined as (choose the best answer):

a) the average propagation delay multiplied by the average power dissipation of a gate,

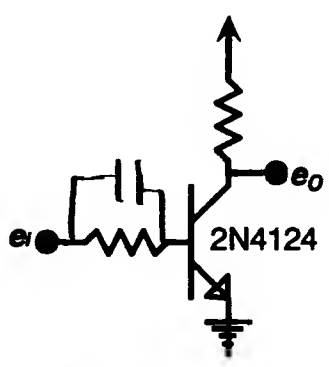
b) the average power consumption of a gate multiplied by the time it is active,

c) the power consumed by a logic gate multiplied by the time it takes for the output to stabilize,

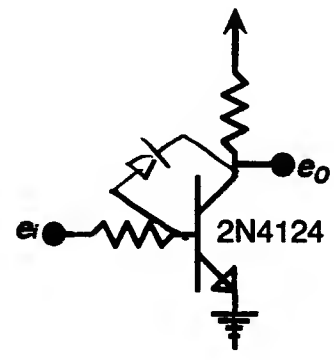
d) the instantaneous power consumed by a gate integrated over the average transition time for the gate (e.g. $\int_0^{t_T} Pdt$).

1

[2] 1.4) Indicate the correct placement of a speed-up capacitor and a bypass diode on the simple transistor inverters shown in the accompanying diagrams.



Speed-up Capacitor



Bypass Diode

2

11

[4] 1.5) **Note:** Do ***either*** part **a)** or part **b)**, ***not both***.

a) Consider the timing requirements for a 7474 dual D-type flip-flop.

t_{Setup} = 20nS
t_{Hold} = 5nS
t_{PHL} – from CLK to Q = 40nS
t_{PLH} – from CLK to Q = 25nS
t_{PHL} – from DC Set / Clear to Q = 40nS
t_{PLH} – from DC Set / Clear to Q = 25nS
$t_{wait(L)}$ – CLK low time = 37nS
$t_{wait(H)}$ – CLK high time = 30nS
$t_{wait(L\ or\ H)}$ – DC Set / Clear = 30nS

i) Assuming Q is low, what is the minimum time that should be allowed after a CLK pulse for Q to change to a high state?

25nS

ii) Assuming Q is high, what is the minimum time that should be allowed after a CLK pulse for Q to change to a low state?

40nS

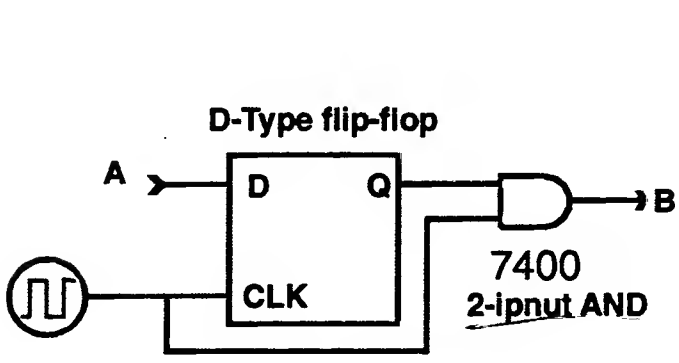
4

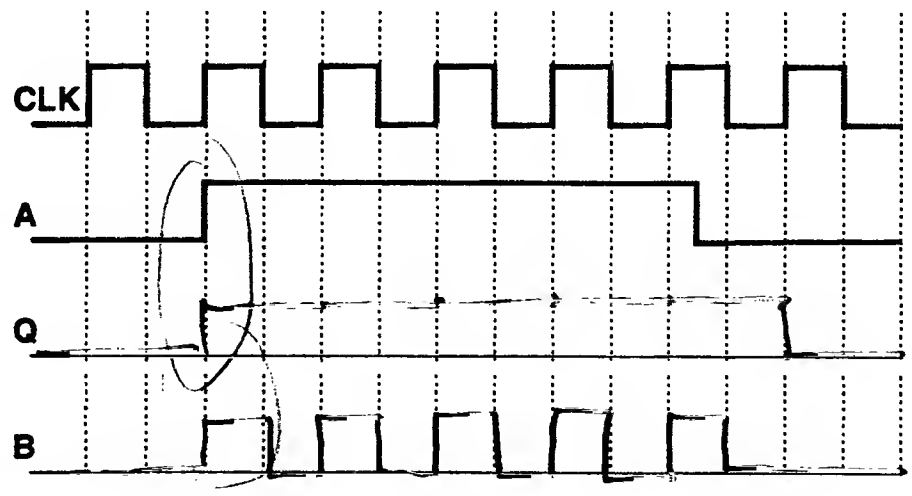
iii) What is the minimum pulse width (in time) that should be applied to the DC Clear input in order to ensure proper operation?

40ns

[4] b) Consider the "touch switch" circuit made using a TTL clock and a D-type flip-flop in the Sequential Logic Laboratory. Explain briefly how a capacitance, C, connected to the CLK input and a resistance, R, connected between the CLK and Q inputs will enable the flip-flop to change state

[4] 1.6) Draw the waveforms for Q and the output, B, for the simple logic circuit shown at right (Assume propagation delays are insignificant and Preset and Clear are set for operation.)





4

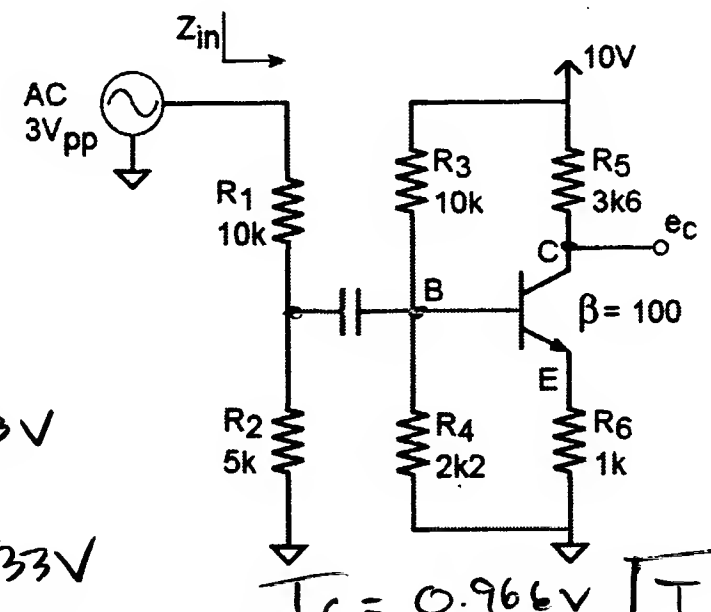
Assume Positive Edge Trigger

Note: There might be an issue indicated (i.e. might not clock in logic 1)

8

BJT Amplifiers

2.1) Use the circuit show at right to answer the following problems. Assume $V_{BE} = 0.7$, $I_C \cong I_E$, and $V_T = 25mV$.



a) Calculate the DC value of the collector current I_C.

[2]

2

$V_B = \frac{R_4}{R_3+R_4}(10V) = \frac{2.2}{12k}(10) = 1.8333V$

$\Rightarrow V_E = 1.833 - 0.7V = 1.133V$

$I_C = \frac{0.966V}{1k}$ $\boxed{I_C = 1.133mA}$

b) Calculate the DC value of the collector-emitter voltage V_{CE}.

[2]

2

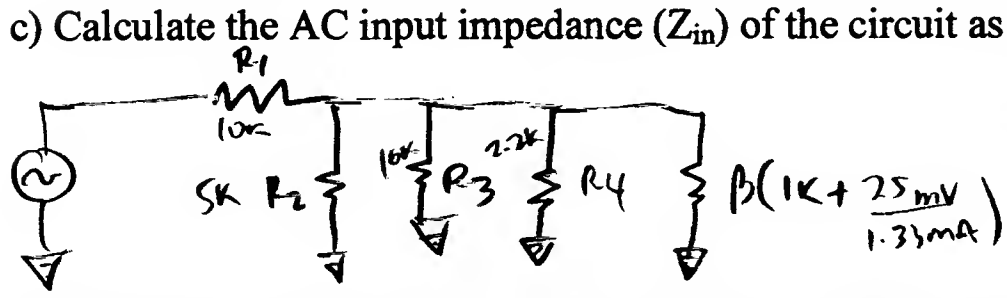
$V_{CE} = V_{CC} - I_C(R_5+R_6)$

$= 10V - (1.133mA)(3.6k+1k)$ $\boxed{V_{CE} = 4.79V}$

c) Calculate the AC input impedance (Z_{in}) of the circuit as seen by the signal source.

[2]

2

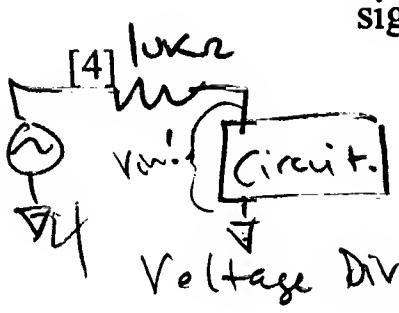


$R_{in} = 10k + 5k \| 2.2k \| 10k \| \beta(1.0\ldots)$

$\boxed{R_{in} = 11.31\ k\Omega}$

d) Calculate the magnitude of the unloaded AC voltage at the collector if the input signal is $3V_{pp}$.

[4]



$Gain = \frac{3.6k}{1K + \frac{25mV}{1.133mA}} = 3.52$

Gain * Input Attenuation

$= 3.52 \times 0.115 = 0.405$

Voltage Divider Attenuation: $\frac{5k \| 2.2k \| 10k \| \beta(1.022)k}{10K + 5k \| 2.2k \| 10k \| \beta(1.022)k} = \frac{1.31}{11.3} = 0.115$

e) Assume that the amplifier drives a load of 5kΩ. Calculate the voltage gain between nodes B and C with the load in place.

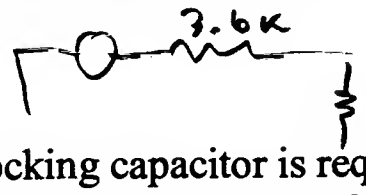
[2]

$(0.405)(3V_{pp}) = \boxed{1.215\ V_{pp}}$

2

$Gain = \frac{3.6K}{1K + \frac{25mV}{1.33mA}} = 3.52$

Attenuation due to Output impedance.



$= \frac{5K}{3.6K+5K} = 0.5814$

3.52×0.5814

$= \boxed{2.05}$ Gain.

[1] 2.2) A blocking capacitor is required at the input of a BJT amplifier in order to

a. increase the gain of the amplifier.
b. eliminate high frequency oscillations.
c. make more work for students.
d. prevent the signal source from shorting the base bias voltage.

1

[2] 2.3) Calculate the minimum value of an input blocking capacitor if the input impedance of the amplifier is Rin = 10 kΩ and the lowest signal frequency is 500 Hz.

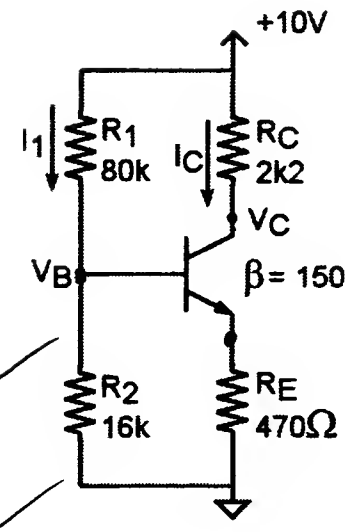
Capacitor Impedance should be <10% that of the input at lowest frequency. $\therefore R_{min} = \frac{1}{2\pi f C} = 1k\Omega$

2

$C = \frac{1}{(1k\Omega)(2\pi)(500)}$

$\boxed{C = 318\ nF\ min}$

2.4) Consider the BJT bias circuit shown at right.



a) The collector current is measured to be $I_C = 2.0\ mA$. Calculate the DC values of I_1, V_B, and V_C.

[3]

$V_C = 10V - 2.0mA(2.2K)$

$V_C = 5.6V$ ✓

Approximation $I_C \simeq I_E$

$V_B = 0.7V + (2.0mA)(470\Omega) = 1.64V$ (V_B) ✓

$I_1 = \frac{10V - 1.64V}{80K} = 0.1045\ mA$ ✓

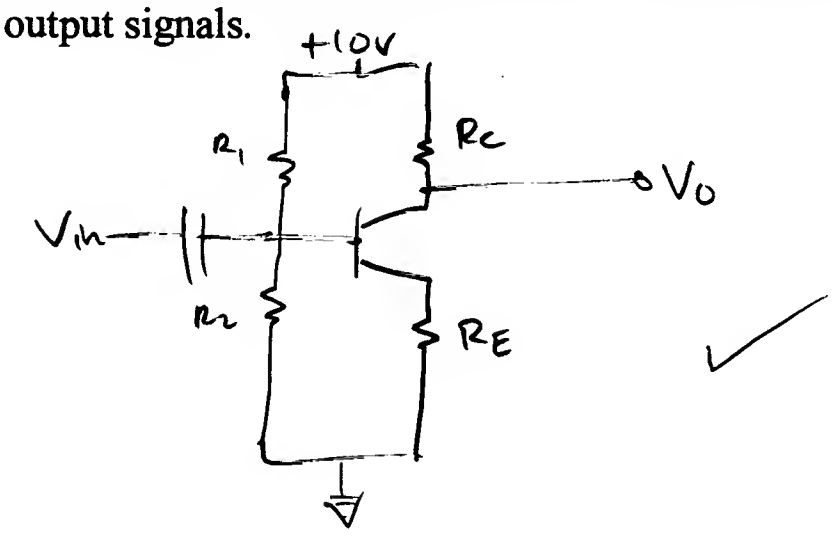
3

b) The circuit shown can be used in one of the following configurations:

i) Common emitter amplifier
ii) Common collector amplifier
iii) Common base amplifier

Redraw the circuit for ***one of*** these configurations with the appropriate input and output signals.

[1]



✓

c) For the configuration chosen in b), calculate the parameters for the amplifier specified below:

i) Common emitter voltage gain A_v, and output impedance R_{out}.
ii) Common collector voltage gain A_v, and input impedance R_{in}.
iii) Common base voltage gain A_v, and input impedance R_{in}.

[2]

$A_v = \frac{R_C}{r_e + R_E}$ $\quad r_e = \frac{V_I}{I_C}$

$R_{IN} = R_1 // R_2 // \beta(r_e + R_E)$ ✓

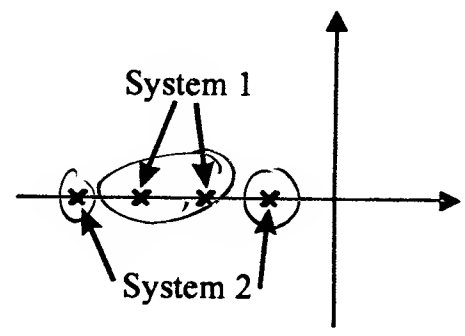
[1] 2.5) A common collector amplifier typically has:

e. Large gain, small R_{in}, small R_{out}
f. Unity gain, large R_{in}, small R_{out} (buffer) ✓
g. Unity gain, small R_{in}, small R_{out}
h. Unity gain, large R_{in}, large R_{out}

Second Order Systems

[2] 3.1) i) Two second order systems have roots as shown in the figure. Which of the following relationships is correct?

a) $\xi_1 > \xi_2$
b) $\xi_1 < \xi_2$
c) $\xi_1 = \xi_2$



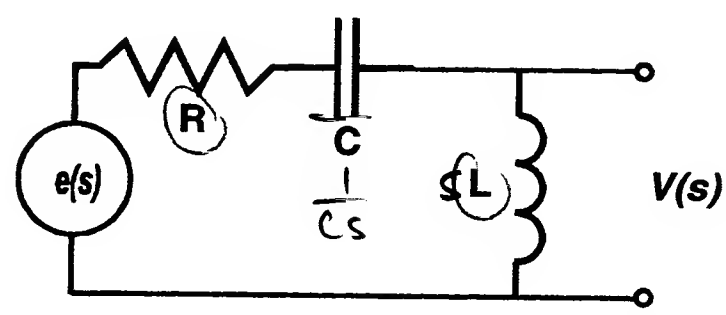
Where ξ_i is the damping factor of system i

ii) Both systems are:
a) critically damped
b) over-damped
c) under-damped

If they were together $\xi = 1$,

∴ farther apart wider. they get, $1 < \xi_1 < \xi_2$

[8] 3.2) For the circuit shown at right, **derive**:
(Assume ideal components)



a) the transfer function $\frac{V(s)}{e(s)}$ in terms of R, L, and C.

$$\frac{V_s}{e_s} = \left(\frac{sL}{sL + \frac{1}{Cs} + R}\right)\left(\frac{Cs}{Cs}\right)$$

$$= \frac{s^2 LC}{s^2 LC + sRC + 1}$$

$$\frac{V(s)}{e(s)} = \boxed{\frac{s^2}{s^2 + s\frac{R}{L} + \frac{1}{LC}}} \checkmark$$

b) the characteristic equation in terms of R, L, and C

$$\boxed{s^2 + s\frac{R}{L} + \frac{1}{LC} = 0} \checkmark$$

c) ω_n, σ, ξ in terms of R, L, and C

$$\boxed{\omega_n = \frac{1}{\sqrt{LC}}} \quad \xi = \frac{\sigma}{\omega_n} \quad \boxed{\sigma = \frac{R}{2L}} \checkmark$$

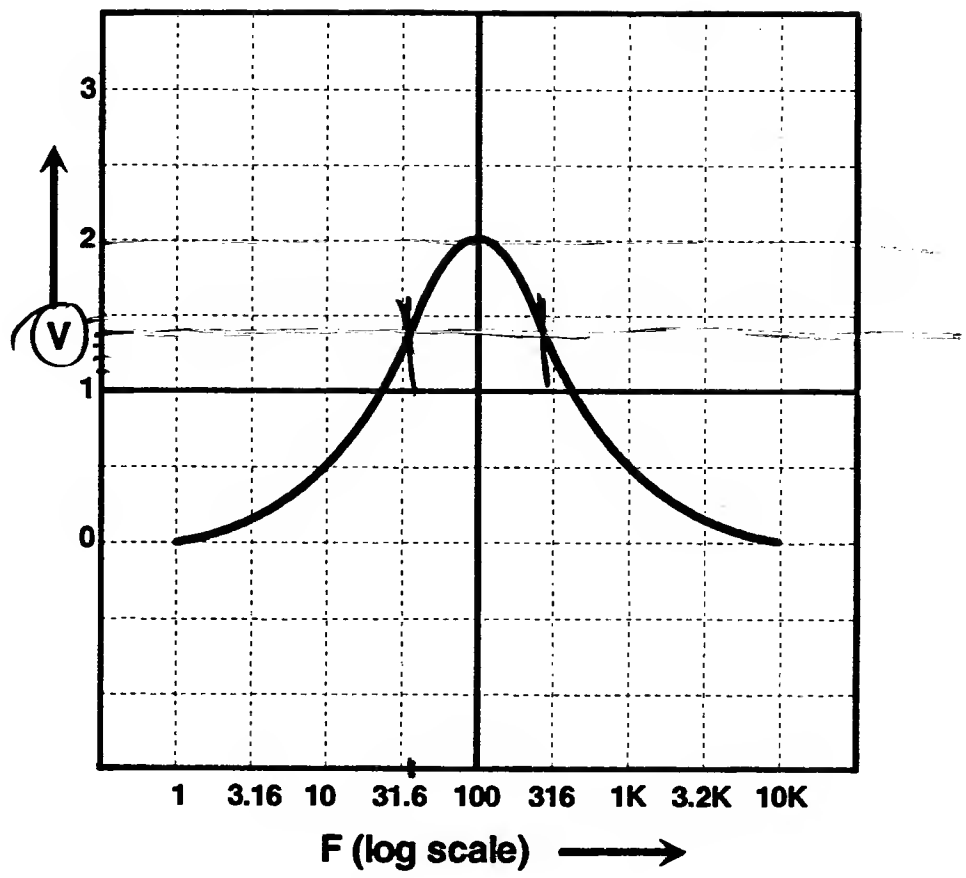
$s^2 + 2\sigma s + \omega_n^2$

$$\xi = \frac{\frac{R}{2L}\sqrt{LC}}{}$$

$$\xi = \frac{\sigma}{\omega_n}$$

$$\boxed{\xi = \frac{R}{2}\sqrt{\frac{C}{L}}} \checkmark$$

3.3) The diagram at right shows a frequency response of a series resonant R-L-C circuit.



[2] a) From this diagram, determine the ½ power bandwidth frequencies (f_1, f_2).

2

Peak = 2V

$\therefore$ 3db down $= \frac{2}{\sqrt{2}} = 1.414$

$f_1 \approx 35$ Hz

$f_2 \approx 300$ Hz

[1] b) If the resistance, R is increased, the centre frequency is

i) increased
ii) decreased ✓
iii) unchanged

1 ideally

(only gets sharper)

3.4) The accompanying graph shows an underdamped system response.

a) What is the percent overshoot (M_p)?

[2]

2

$\frac{\Delta V_2}{\Delta V_1} = \frac{0.6V}{2.5V}$

$= 0.24$ ✓

$= 24\%$

b) What is the damping factor (ξ)?

[2]

1.5

$\zeta = \sqrt{\frac{[\ln(M_p)]^2}{\pi + [\ln(M_p)]^2}}$

$\zeta = 0.564$ | too big (-.5)

c) Find the roots for this system ($s_1, s_2 = -\sigma \pm j\omega_d$)

[4]

3.5

$\sigma = \frac{\ln\left(\frac{V_2}{V_2}\right)}{\Delta t} = \frac{\ln\left(\frac{0.4V}{0.6V}\right)}{200ns} = 2027$ krad/s ✓

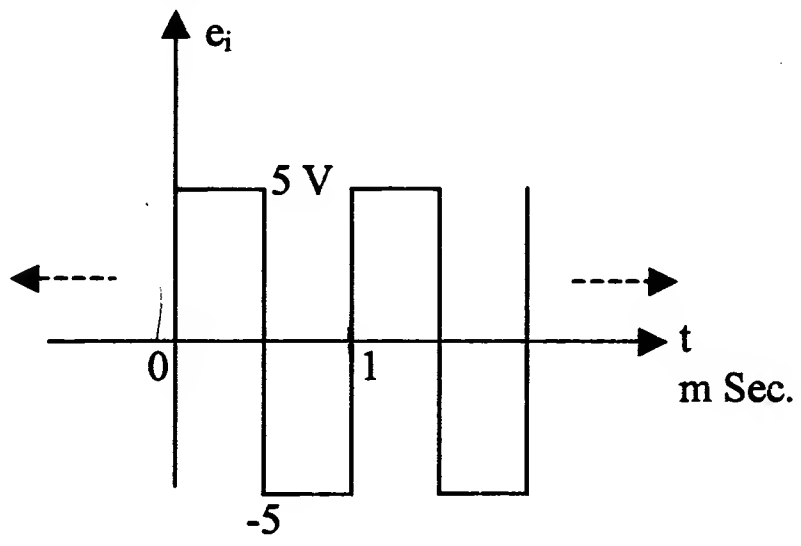
$\omega_d = \frac{1}{\Delta t} 2\pi = \frac{2\pi}{200ns} = 31.4 \times 10^6$ krad/s ✓ almost!

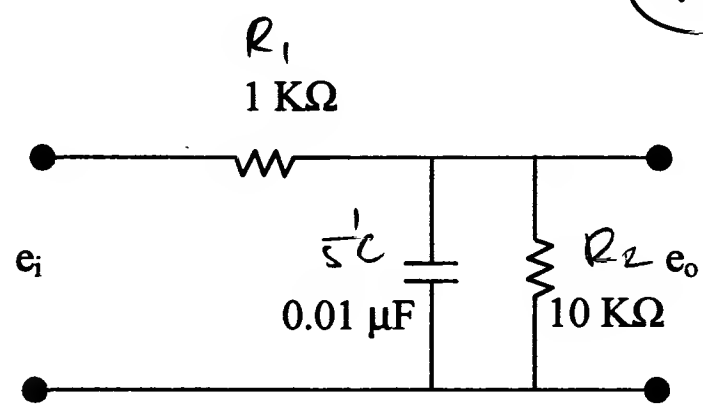
$s_1, s_2 = -2027 \pm 31.4^{\times 10^6}$ krad/s (-.5)

Fourier Analysis

10

4.1) Consider the input waveform and circuit shown below:





[6] a) The input voltage e_i is a square wave of 10 Vp-p. Predict the 3rd harmonic components of the output wave form in rms.

[3] b) What type of filter is this circuit?

[1] c) Sketch the output wave form e_o.

Input.

a) Signal: $\frac{4V_p}{n\pi}$ ✓

$f_0 = \frac{1}{1ms} = 1kHz$

$3f_0 = 3kHz.$

$\therefore e_o = \frac{(0.896)(4)(5)}{(3)(\pi)}$ ✓

$= 1.9014$ peak

$* \frac{1}{\sqrt{2}} = \boxed{1.34\ V_{rms}}$

$\frac{V_o}{V_{in}} = \frac{\frac{R_2}{sC}}{\frac{1}{sC} + R_2}$

$\frac{V_o}{V_{in}} = \frac{\frac{R_2}{sC}}{R_1 + \frac{R_2}{sC}}$

$\frac{V_o}{V_{in}} = \frac{\frac{R_2}{sC}}{\frac{1}{\frac{1}{sC} + R_2}}$

$\frac{V_o}{V_{in}} = \frac{\frac{R_2}{sC}}{R_1 R_2 + \frac{R_1}{sC} + \frac{R_2}{sC}}$

$= \boxed{\frac{R_2}{sR_1R_2C + (R_1 + R_2)}}$

@ 3kHz:

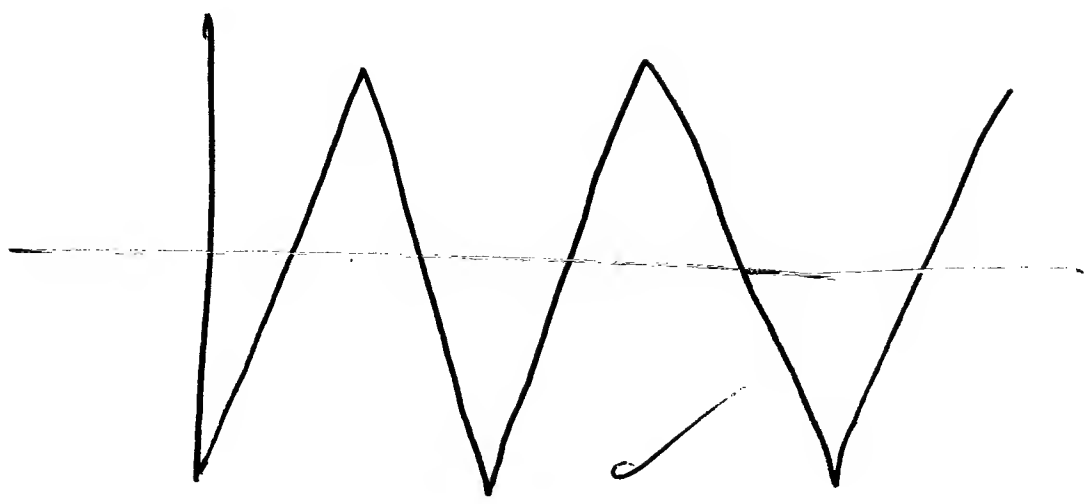
$\frac{10k\Omega}{j(2\pi)(3kHz)(10k\Omega)(N/\Omega)(0.01\mu F) + (10k\Omega + 1k\Omega)}$

$= \frac{|10k\Omega|}{|j1884.95 + 11000|}$

$= 0.896$ ✓

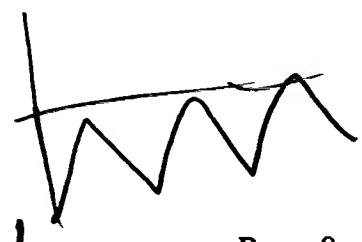
(b) Low Pass ✓
$f \to \infty \quad H(s) \to 0$

(c)



Integral.

maybe Dc offset!

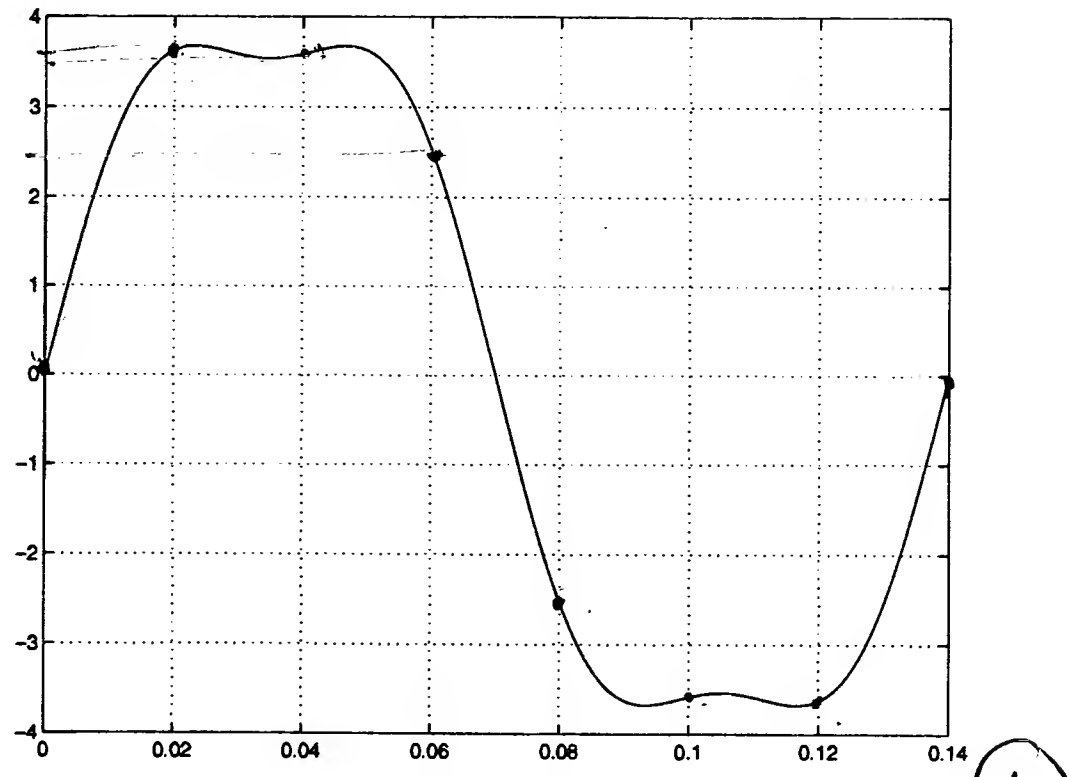


$\left(\frac{2\pi n i}{N}\right)$

4.2)

[8] a) Find the 3rd harmonic component in rms of the following wave form using DFT.

Use $\Delta t = 0.02$ sec. i.e.(8 samples)



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$n=3$

Δt	t_i	w_i	cos	sin	f_{cos}	f_{sin}	
0.02	0	0	1 ✓	0	0	0	1
0.04	3.6	1	-0.707	0.707	-2.545	2.545	2
0.04	3.5	2	0	-1	0 ✓	-3.5 ✗	3
0.06	2.5	3	0.707	0.707	1.7987	1.7887	4
0.08	2.5	4	-1	0	2.54	0	5
0.10	3.5	5	0.707	-0.707	-2.475	2.475	6
							7
0.12	3.6	6	0	1	0	3.6	
0.14	0	7	0	0	+0.69	←	8 ?

$\bar{4}$

$= 0.0864$ a_3

$0.86 \Rightarrow \sqrt{a^2 + b^2} = 0.865$

b_3 α α

[2] b) Compare the 3rd harmonic component calculated using DFT with the exact value (0.5 volt).

Note: the wave form is $V = \sqrt{2}\cdot(3)\sin(2\pi f\cdot t)+\sqrt{2}\cdot(0.5)\sin(2\pi f\cdot 3\cdot t)$

Where: f = 1/0.14 Hz, this formula maybe used to find the samples values.

Only third $\cdot (\sqrt{2})(0.5)(\sin 2\pi f 3t)$

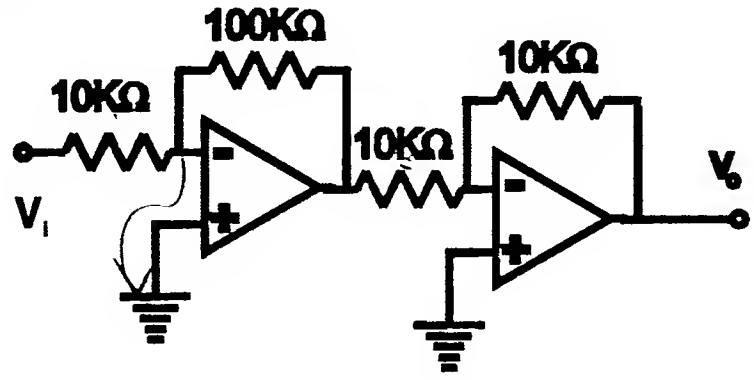
different

$= 0.306$

2

Operational Amplifiers

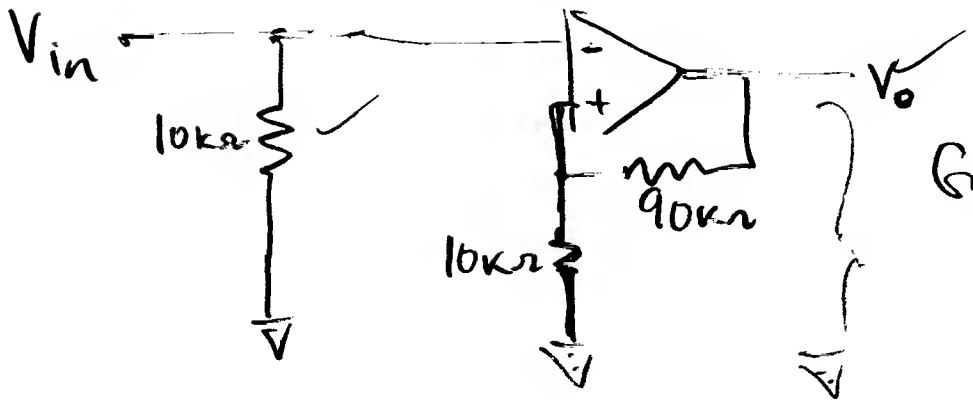
[4] 5.1) Determine the input impedance, Z_{in}, and the voltage gain, A_v for the following operational amplifier circuit.



Z_{in} 10 kΩ ✓ A_v Cascade = +10 ✓

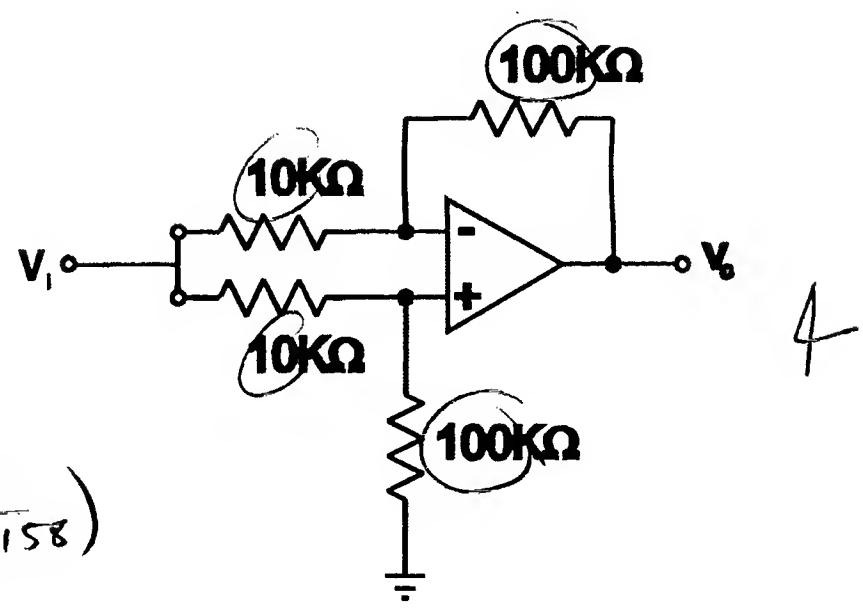
Design a circuit with the same Z_{in} and A_v but using only *one* OP Amp.

4



$$\text{Gain} = \left(1 + \frac{90}{10k\Omega}\right) = 1+9 = 10 \checkmark$$

[4] 5.2) The circuit at right is set up to measure the common mode gain. The input signal, $v_i = 10\sin(3770t)V$, and the output, v_o is measured to be $158.7\sin(3770t)mV$. Calculate the Common-mode Rejection Ratio (CMMR) in db. (**Note:** Assume all resistance are perfect values - i.e. no tolerance)



4

CMMR: 56 dB

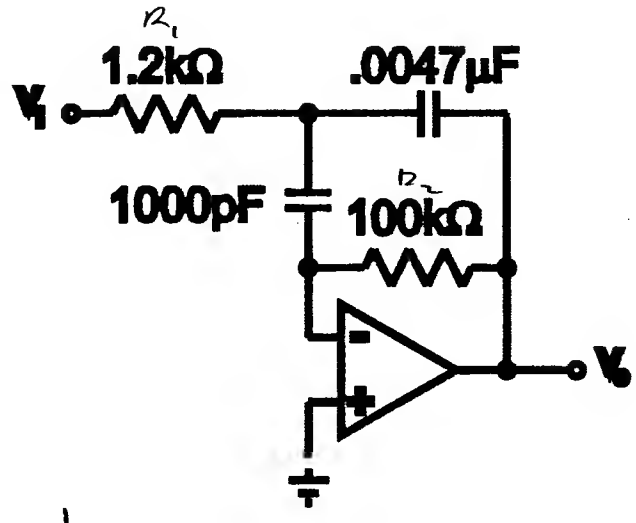
Diff mode Gain = 10. $20\log\left(\frac{10}{0.0158}\right)$

Common mode Gain = $\frac{0.158}{10} = 0.0158$

[4] 5.3) Given the op-amp active filter at right, calculate:

i) the expected Quality Factor, Q: 5.45 X 1

ii) the centre frequency, f_o in Hz: 6702 Hz ✓



3

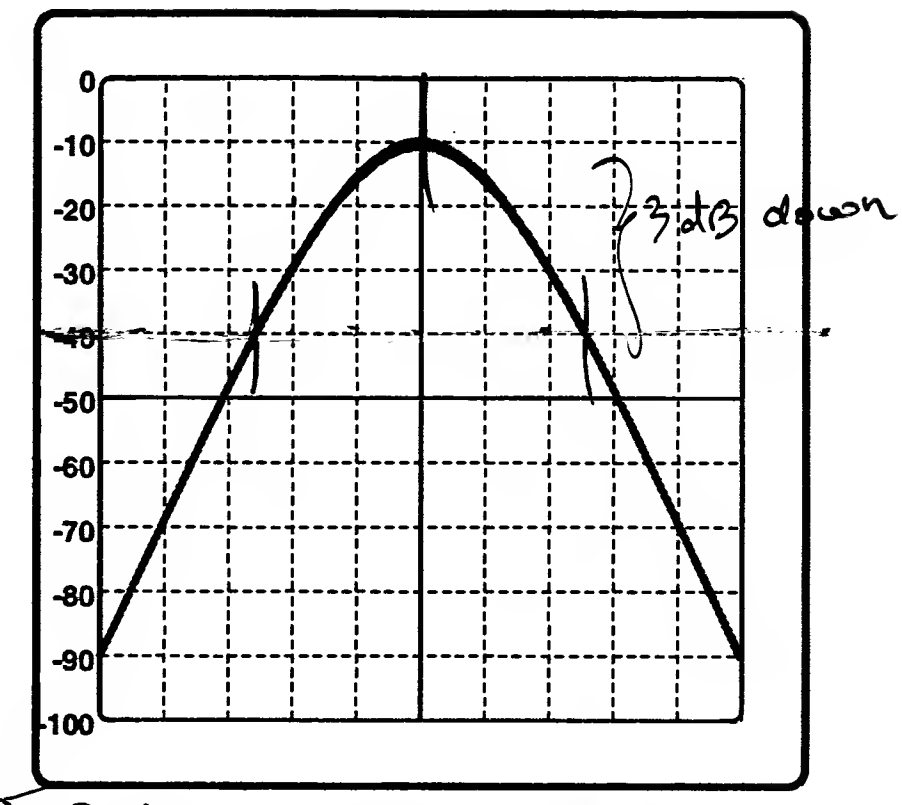
(i) $Q = \checkmark \frac{f_o}{BW} = \frac{6701.6\,Hz}{1.23\,kHz}$

$$f_o = \frac{1}{2\pi\sqrt{C_1 C_2 R_1 R_2}} = \frac{1}{2\pi\sqrt{(1000\times10^{-12})(0.0047\times10^{-6})(1.2k\Omega)(100k\Omega)}}$$

$f_o = 6701.6\,Hz$ ✓

11

[5] 5.4) The output of an active filter is shown on the HP3580A Spectrum Analyzer display pictured at right. The settings on the instrument were as follows:



Vertical settings:
- Scale: 1db/div
- sensitivity: -10db

Horizontal Settings:
- Resolution Bandwidth: 30Hz
- Freq span/div: .2kHz
- Centre Frequency: 4739Hz
- Sweep Rate: .2S/div

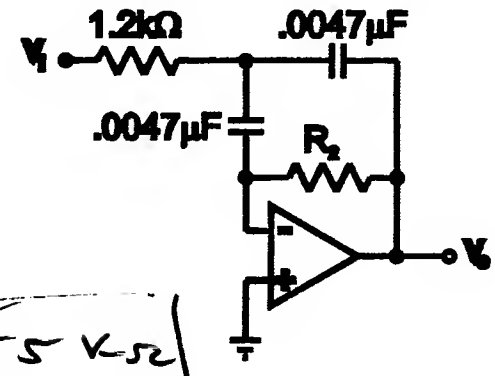
i) What is the bandwidth of this filter?

5 div × .2kHz = 1kHz

ii) What is the Quality Factor, Q?

$Q = \frac{f_o}{BW} = \frac{4739}{1kHz} = 4.739$ Hz

iii) If this filter is implemented using the op-amp circuit shown at right, calculate the value of the resistor, R_2.



$f_o = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$

$R_2 = 42550\ \Omega$ $R_2 = 42.55\ k\Omega$

[1] 5.5) In the lab you measured a property of non-ideal op-amps called the slew rate. What does this value refer to?

1) The maximum frequency of the input signal when the input signal is a square wave.
2) The maximum rate of change of the output voltage.
3) The bandwidth of the op-amp.
4) How fast the op-amp can charge a capacitive load.

[2] 5.6) A non-inverting amplifier is designed to have a voltage gain of 40dB. The unity gain bandwidth of the op-amp used to build the circuit is 3 MHz. What is the bandwidth of the amplifier?

1) 75 kHz
2) 300 Hz
3) 6 kHz
4) 30 kHz

$20\log(\text{gain}) = 40$

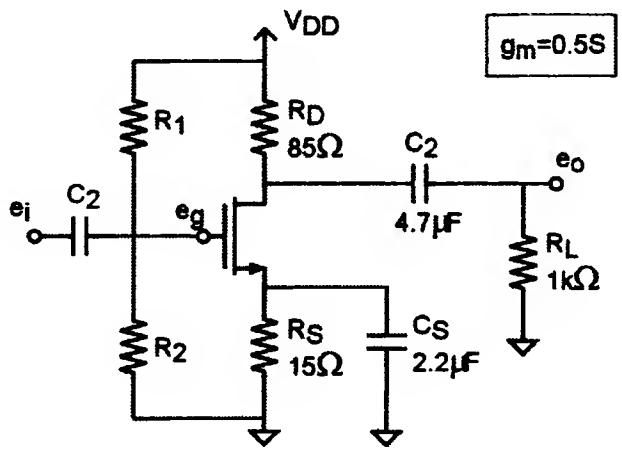
$40\text{dB} \Rightarrow 10^{\frac{40}{20}} = 100$ Gain.

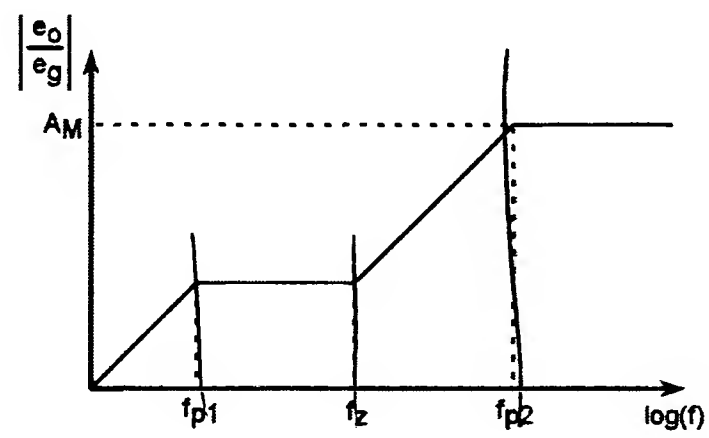
$\therefore \frac{3\text{MHz}}{100} = 30\text{kHz}$

8

FET Amplifiers

[6] 6.1) The frequency response of the FET amplifier shown below is sketched in the attached graph. Note that the input signal has been measured at the gate of the FET.





a) What is the output impedance R_{out} of the amplifier?

$R_D = 85\,\Omega$ ✓

2

b) Calculate the values for the break frequencies f_{p1}, f_z, and f_{p2}.

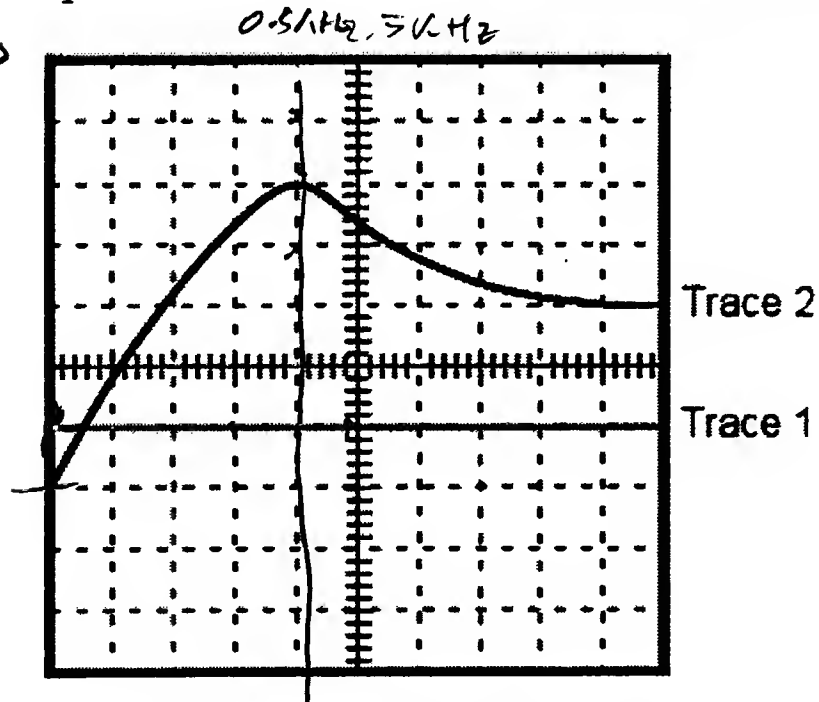
$f_{p1} = \frac{1}{2\pi C_1 R_{in}}$ $f_z = \frac{1}{2\pi C_S R_S}$ $f_{p2} = \frac{1}{C_2 R_{||}(\frac{1}{g_m}) \times 2\pi}$ ~~0.5~~ 1.

c) Calculate the value of the gain A_M above frequency f_{p2}?

$A_m = g_m R_D = (0.5)(85) = 42.5$ X.

[4] 6.2) The frequency response of a circuit is measured using the HP3580A Spectrum Analyzer (see attached sketch). Trace 1 shows the magnitude of the tracking oscillator signal. The tracking oscillator signal is fed into the input of the circuit and trace 2 is measured at the output of the circuit. The relevant instrument settings are listed in the table.

+20 0.5kHz, 5kHz



Vertical settings:
Scale: 10 dB/div
Sensitivity: +20

Horizontal settings:
Resolution Bandwidth: 30 Hz
Freq Span / div: 0.5 kHz
Center Freq: 2.5 kHz

a) What is the frequency of the resonant peak?

2 kHz ✓

b) What is the circuit gain at the peak frequency?

3

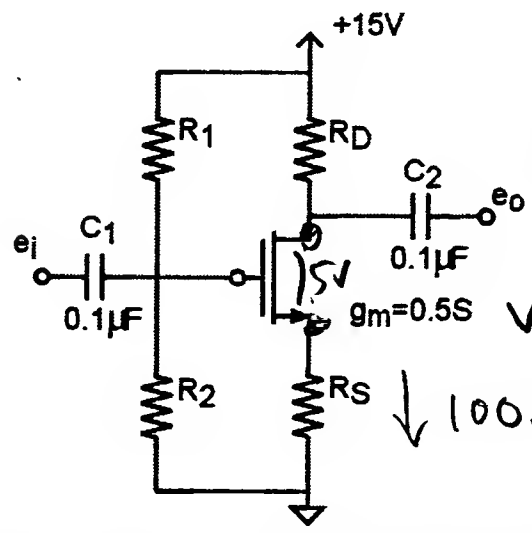
$10dB * 4 = \boxed{40\,dB} = 100$ ✓

c) What is the circuit gain at a frequency of 5 kHz?

$\boxed{-10\,dB} = 0.316$ X.

5

[6] 6.3) Consider the FET bias circuit shown below.



I_D = 100 mA
V_{DS} = 5 V
V_{GS} = 2.5 V

$V_S = 15 - (0.100)(50) - (5)$

↓ 100mA $V_S = 5$.

a) Determine the values of R_1, R_2, R_D and R_S to achieve an output impedance of 50 Ω and an input impedance of 50 kΩ.

$R_D = 50\Omega$ ✓

$R_1 // R_2 = 50\,k\Omega$. $\frac{R_1 R_2}{R_1 + R_2} = 50 \times 10^3$

AND $\left(\frac{R_2}{R_1 + R_2}\right) 15V = 2.5V + 5$

$V_S = 5V$

3.5

$\therefore R_S = \frac{5V}{100mA}$ $R_S = 50\Omega$ ✓

$\frac{R_2}{R_1 + R_2} = \frac{7.5}{15}$

b) Calculate the unloaded voltage gain of this amplifier?

$\frac{-R_D}{\frac{1}{g_m} + R_S}$ $\frac{-50}{2+50} = -0.9615$ ✓

c) The frequency response of the unloaded circuit is to be measured using an oscilloscope probe at the output of the amplifier. Calculate the expected low frequency cutoff of the amplifier.

$f_{cutoff_{low}} = \frac{-1}{2\pi C_1 R_{in}}$ 0.5

d) Based on your experience in the lab, what must be connected between the tracking oscillator output and the circuit input in order to measure the frequency response with the Spectrum Analyzer.

buffer! tracking oscillator ✓

[2] 6.4) Describe the methods used to measure the input and output impedance of the FET amplifier.

- Measure unloaded output voltage, Add series load, adjust until ½ original voltage, $R_{Load} = R_{out}$ ✓
- Same process but with series input. ✓

2.

5.5